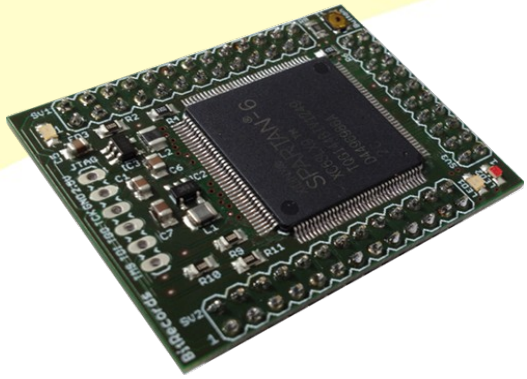
BitRecords FPGA Module XC6SLX9



FPGA module for use in the fields of hobby and prototyping

Characteristics:

- Xilinx Spartan 6 (XC6SLX9-2TQG144C)
- 68 User IOs
- 2 LEDs, 1 PushButton
- On-board 50MHz oscillator
- Voltage Feed: 3.3V
- SPI Flash for configuration and user data storage
- 6-Pin JTAG Header
- Grid Dimension: 2.54 mm
- Size: 46 x 36 mm

Supply Voltages:

For operation of the FPGA module, a voltage feed of 3.3V is neccessary, which can be supplied via the connection headers (see Pin Assignments).

The operating voltages of all FPGA banks and user IOs is set to 3.3V.

On-Board Interfaces:

Two user LEDs (active high) and one PushButton (active low) are mounted on the module as well as a 50MHz oscillator for synchronous FPGA operations. The following FPGA pins are used:

LED1 – P1 (FPGA Pin)
LED2 – P2
Taster – P35
50MHz – P14

Flash storage:

The mounted 32MBit SPI Flash (Nymonyx M25P32) can be used to store the FPGA start-up files as well as user data of the running system.

The following FPGA pins are used to connect the Flash:

D (Serial Data Input) – P64 (FPGA-Pin)
Q (Serial Data Output) – P65

C (Serial Clock) – P70
S(Chip Select) – P38

The Flash signals $\overline{W}$ und $\overline{HOLD}$ are permanently tied to HIGH.

Configuration:

The configuration of the module is implemented via a 6-Pin JTAG header, which can be used to transfer the parameter files directly to the FPGA SRAM (for test purposes) or to the connected SPI Flash storage (automatically loaded at start-up after power supply). This programming can be done by the Xilinx iMPACT Tool, for example.

A successfull configuration is shown by an glowing DONE LED.

To store the parameter files into the Flash, an indirect SPI programming is used. A detailed tutorial is given in Appendix B.

Pin Assignments:

The following FPGA pins are connected to the three connection headers:

S1

GND	1	2		**3.3V**
P81	3	4		P80
P79	5	6		**P78**
P74	7	8		P75
P67	9	10		**P66**
P62	11	12		P61
P59	13	14		**P58**
P57	15	16		P56
P55	17	18		**P51**
P50	19	20		P47
P45	21	22		**P46**
P43	23	24		P44
P40	25	26		**P41**

S2

3.3V	1	2		**GND**
P94	3	4		P93
P98	5	6		**P97**
P100	7	8		P101
P112	9	10		**P111**
P115	11	12		P114
P117	13	14		**P116**
P124	15	16		P123
P127	17	18		**P126**
P133	19	20		P132
P138	21	22		**P137**
P140	23	24		P141
P142	25	26		**P143**

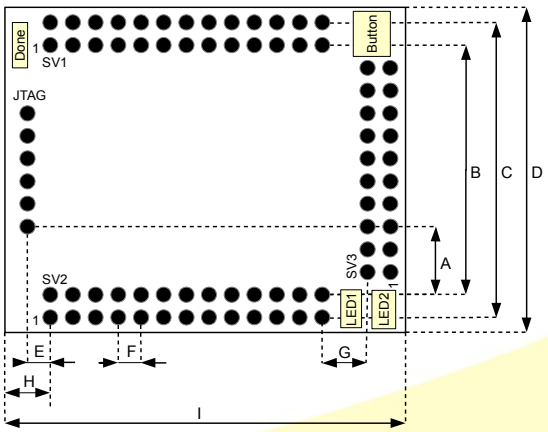
S3

P6	1	2		**P5**
P9	3	4		P7
P10	5	6		**P8**
P12	7	8		P11
P17	9	10		**P16**
P23	11	12		P22
P24	13	14		**P26**
P27	15	16		P30
P29	17	18		**P33**
P32	19	20		P34

The detailed pin descriptions are given in Appendix A.

Dimensions:

Symbol	Measure (mm)
A	7.62
B	27.94
C	33.02
D	36.07
E	2.54
F	2.54
G	3.81
H	6.10
I	45.72



Appendix A: PinOut

SV1

Header	FPGA		
Pin #	Pin #	Bank	Pin Description
1	GND		
2	3.3V		
3	P81	1	IO_L46P_1
4	P80	1	IO_L46N_1
5	P79	1	IO_L47P_1
6	P78	1	IO_L47N_1
7	P74	1	IO_L74N_1
8	P75	1	IO_L74P_1
9	P67	2	IO_L2P_2
10	P66	2	IO_L2N_2
11	P62	2	IO_L12P_2
12	P61	2	IO_L12N_2
13	P59	2	IO_L13N_2
14	P58	2	IO_L14P_2
15	P57	2	IO_L14N_2
16	P56	2	IO_L30P_GCLK1_2
17	P55	2	IO_L30N_GCLK0_2
18	P51	2	IO_L31P_GCLK31_2
19	P50	2	IO_L31N_GCLK30_2
20	P47	2	IO_L48N_2
21	P45	2	IO_L49N_2
22	P46	2	IO_L49P_2
23	P43	2	IO_L62N_2
24	P44	2	IO_L62P_2
25	P40	2	IO_L64N_2
26	P41	2	IO_L64P_2

SV2

Header	FPGA		
Pin #	Pin #	Bank	Pin Description
1	3.3V		
2	GND		
3	P94	1	IO_L40N_GCLK10_1
4	P93	1	IO_L41P_GCLK9_1
5	P98	1	IO_L34P_1
6	P97	1	IO_L34N_1
7	P100	1	IO_L33P_1
8	P101	1	IO_L32N_1
9	P112	0	IO_L66P_SCP1_0
10	P111	0	IO_L66N_SCP0_0
11	P115	0	IO_L65P_SCP3_0
12	P114	0	IO_L65N_SCP2_0
13	P117	0	IO_L64P_SCP5_0
14	P116	0	IO_L64N_SCP4_0
15	P124	0	IO_L37P_GCLK13_0
16	P123	0	IO_L37N_GCLK12_0
17	P127	0	IO_L36P_GCLK15_0
18	P126	0	IO_L36N_GCLK14_0
19	P133	0	IO_L34N_GCLK18_0
20	P132	0	IO_L35P_GCLK17_0
21	P138	0	IO_L4P_0
22	P137	0	IO_L4N_0
23	P140	0	IO_L3P_0
24	P141	0	IO_L2N_0
25	P142	0	IO_L2P_0
26	P143	0	IO_L1N_VREF_0

SV3

Header	FPGA		
Pin #	Pin #	Bank	Pin Description
1	P6	3	IO_L52P_3
2	P5	3	IO_L52N_3
3	P9	3	IO_L50N_3
4	P7	3	IO_L51N_3
5	P10	3	IO_L50P_3
6	P8	3	IO_L51P_3
7	P12	3	IO_L49P_3
8	P11	3	IO_L49N_3
9	P17	3	IO_L43P_GCLK23_3
10	P16	3	IO_L43N_GCLK22_3
11	P23	3	IO_L41N_GCLK26_3
12	P22	3	IO_L42P_GCLK25_3
13	P24	3	IO_L41P_GCLK27_3
14	P26	3	IO_L37N_3
15	P27	3	IO_L37P_3
16	P30	3	IO_L36P_3
17	P29	3	IO_L36N_3
18	P33	3	IO_L2P_3
19	P32	3	IO_L2N_3
20	P34	3	IO_L1N_3

OnBoard

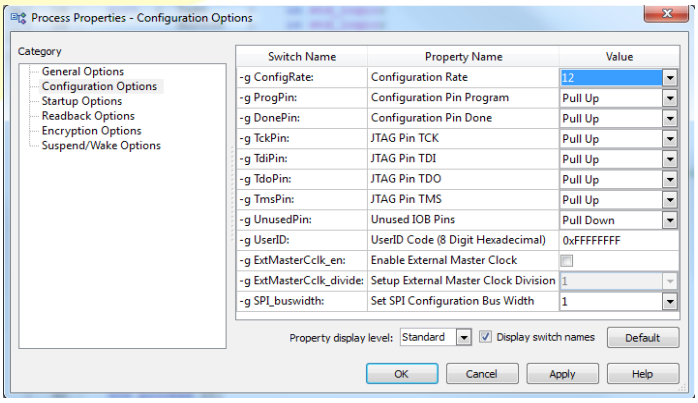
Signal	Pin #	Bank	Pin Description
LED1	P1	3	IO_L83N_3
LED2	P2	3	IO_L83P_3
Taster	P35	3	IO_L1P_3
50MHz	P14	3	IO_L44N_GCLK20_3

Flash

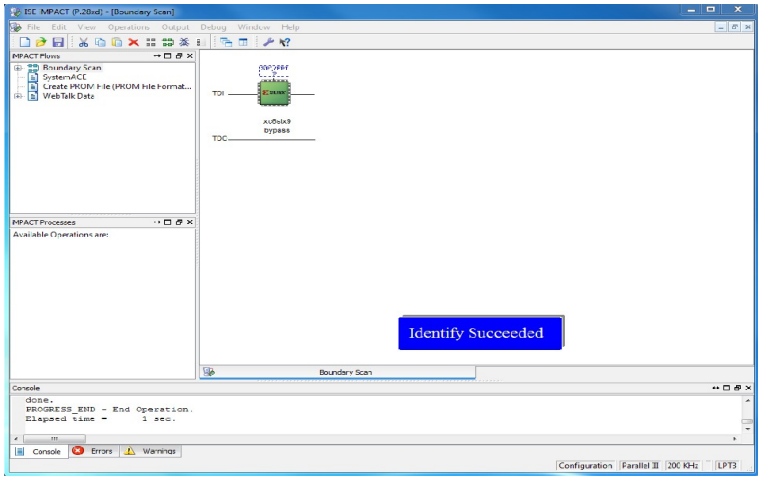
D	P64	2	IO_L3N_MOSI_2
Q	P65	2	IO_L3P_DIN_2
C	P70	2	IO_L1P_CCLK_2
$\overline{S}$	P38	2	IO_L65N_CSO_B_2

Appendix B: SPI Flash configuration (Xilinx iMPACT)

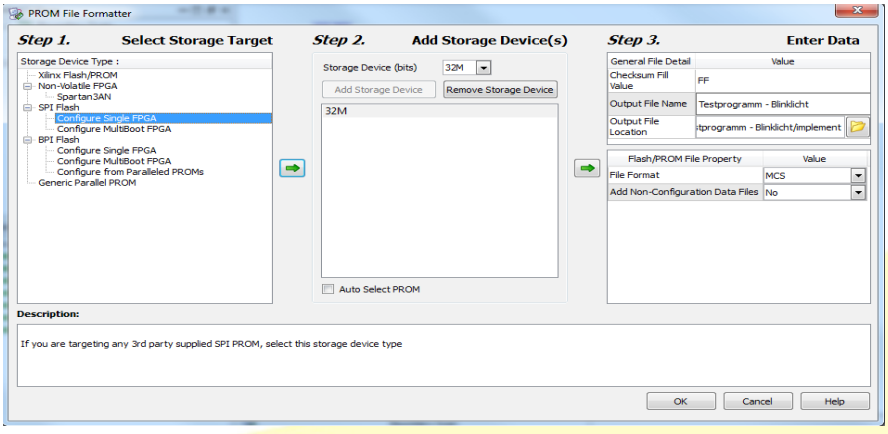
- if you are using the Xilinx ISE Project Navigator to generate the FPGA bit files , select the configuration rate for the SPI Flash PROM as followed:
  Generate Programming File → Process Properties → Configuration Options → Configuration Rate → 12



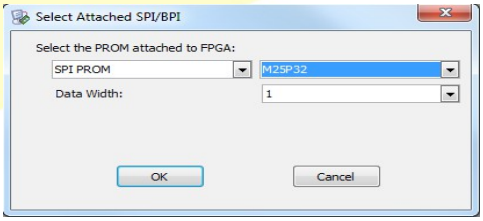
- connect the module via the JTAG pins to the computer and check, that the power supply is established correctly
- start the Xilinx iMPACT tool and select the Boundary Scan Modus
- the Xilinx Spartan 6 FPGA should now be identified



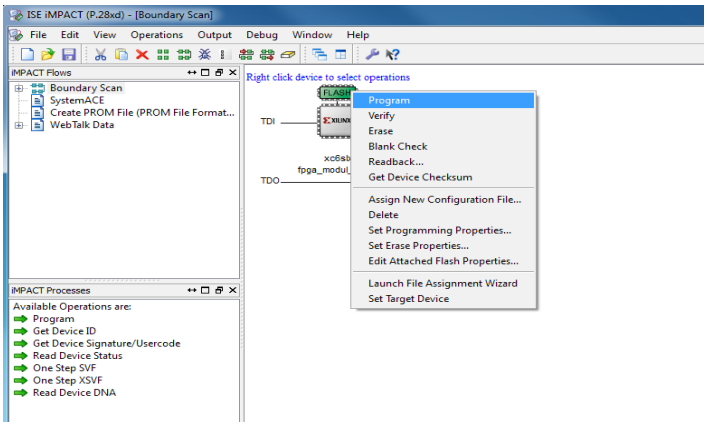
- generate an mcs configuration file for the Flash storage; select the „Configure Single FPGA“ option and 32MBit as the storage device (bits)



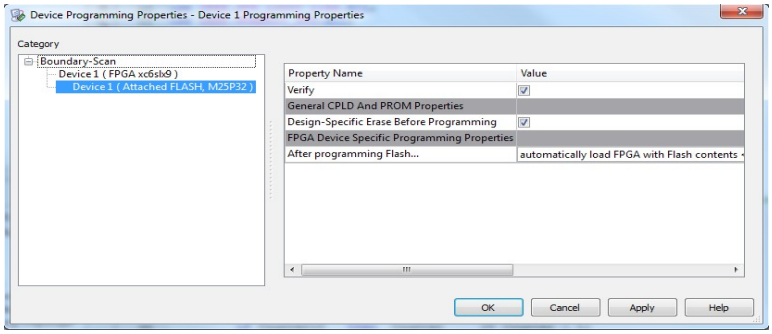
- select the option „Add SPI/BPI Flash ...“ after right-click on the FPGA-Icon and the mcs file in the pop-up dialog
- select the correct SPI Flash (SPI PROM – M25P32)



- start the programming by select the „Program“-Option after right-click on the Flash-Icon



- select the properties „Verify“ and „Erase before Programming“



- after a correct file transfer, the storaged file is automatically loaded into the FPGA SRAM within the start-up process after the power supply is established