Nexys4 Hardware

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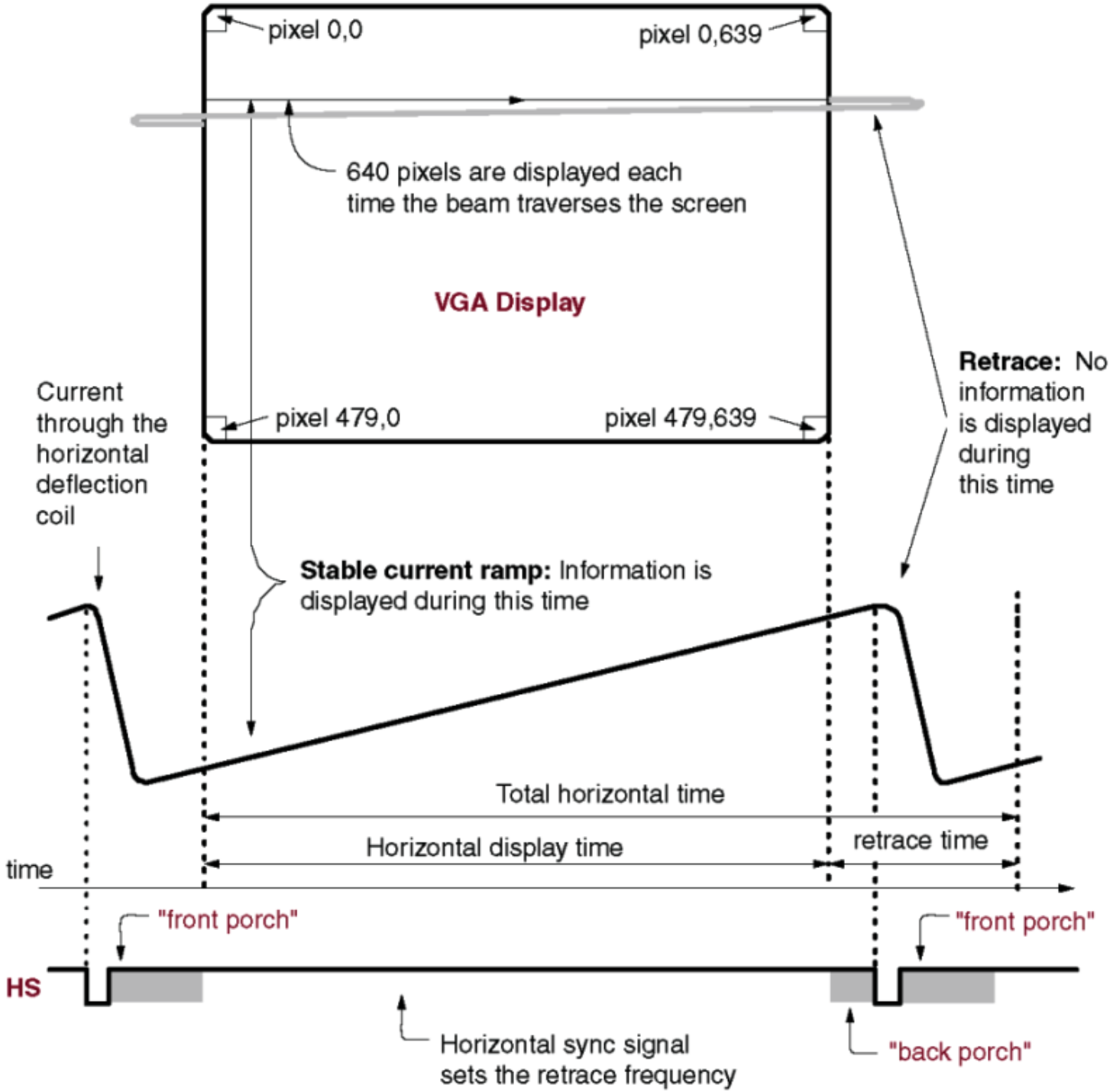
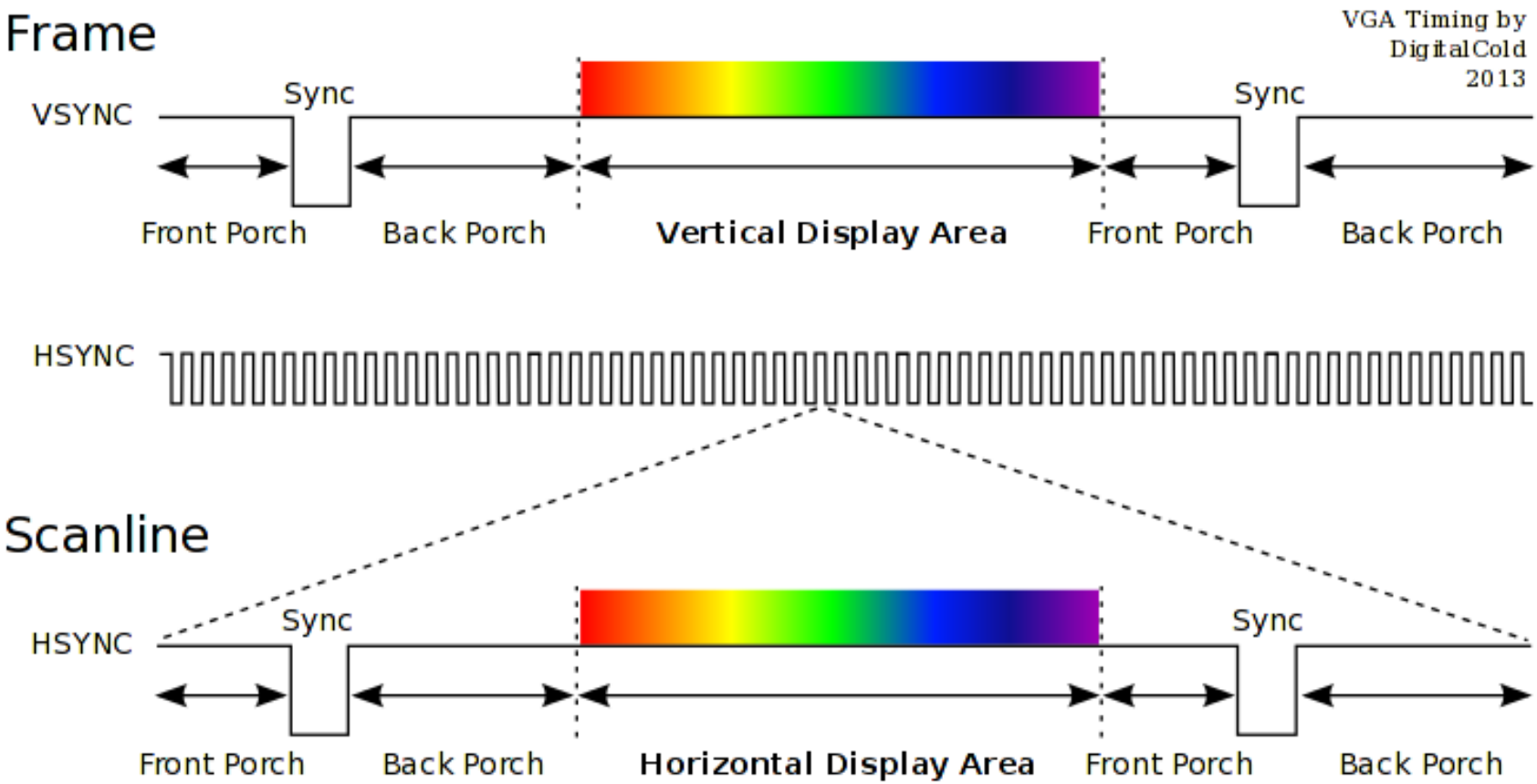

pixel 0,0
pixel 0,639
640 pixels are displayed each time the beam traverses the screen
VGA Display
pixel 479,0
pixel 479,639
Current through the horizontal deflection coil
Retrace: No information is displayed during this time
Stable current ramp: Information is displayed during this time
Total horizontal time
Horizontal display time
retrace time
time
"front porch"
"front porch"
HS
Horizontal sync signal sets the retrace frequency
"back porch"


Frame
VGA Timing by
DigitalCold
2013
VSYNC
Sync
Sync
Front Porch
Back Porch
Vertical Display Area
Front Porch
Back Porch
HSYNC
Scanline
HSYNC
Sync
Sync
Front Porch
Back Porch
Horizontal Display Area
Front Porch
Back Porch

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Timing:
`http://tinyvga.com/vga-timing`

Minimalbeispiel:
- 640x480@60Hz mit 25MHz Pixeltakt
- generiert Sync-Signale
- malt ein weißes Rechteck

Code:
`http://nas.gus.tl/fpga/nexys4_vga_minimal.zip`

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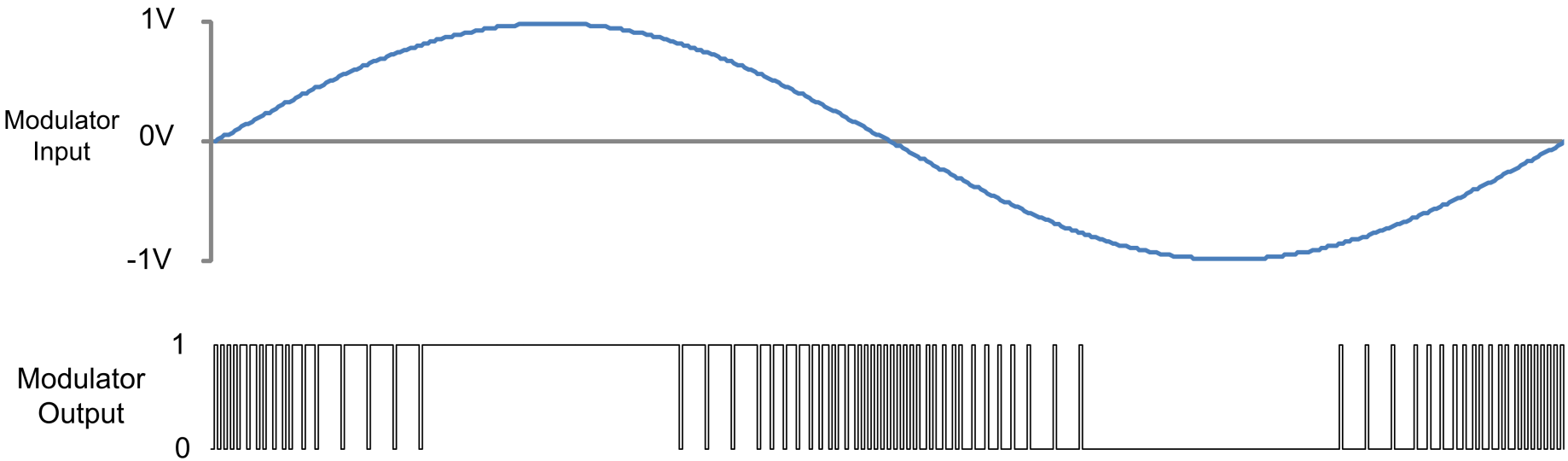
Datenblatt:

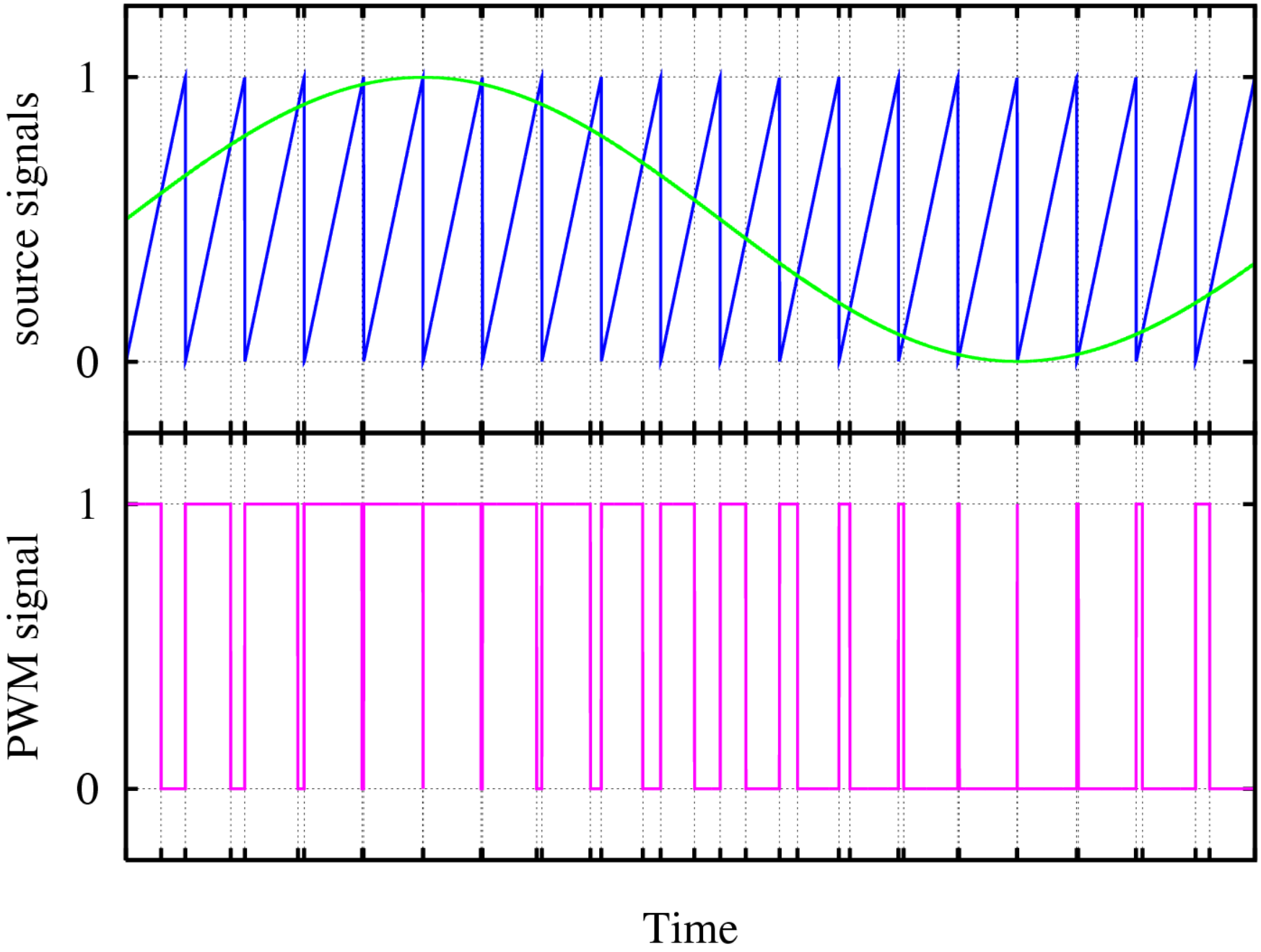
`http://www.analog.com/media/en/technical-documentation/obsolete-data-sheets/ADMP421.pdf`



```
begin

micClk <= mic_clk;
micLRSel <= '0';

process begin
wait until falling_edge(mic_clk);
    sr <= sr(254 downto 0) & micData;
    if    sr(255) = '1' and sr(0) = '0' then
        mic_byte <= mic_byte -1;
    elsif sr(255) = '0' and sr(0) = '1' then
        mic_byte <= mic_byte +1;
    end if;
end process;
```


source signals
1
0
PWM signal
1
0
Time

```
begin

ampSD <= '1';

process begin
    wait until falling_edge(clk);
    pwm_counter <= pwm_counter +1;

    if pwm_counter = 0 then
        pwm_byte <= Wert;
    end if;

    if pwm_counter < pwm_byte then
        ampPWM <= '1';
    else
        ampPWM <= '0';
    end if;
end process;
```

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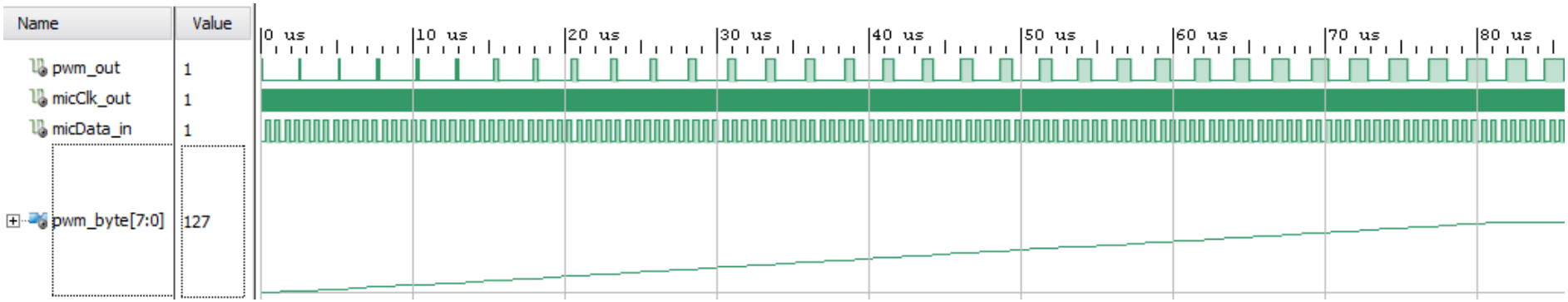
Minimalbeispiel:

- Mikrofon (PDM) => Audio Out (PWM)
- 8-Bit Audio, Mono

Code:

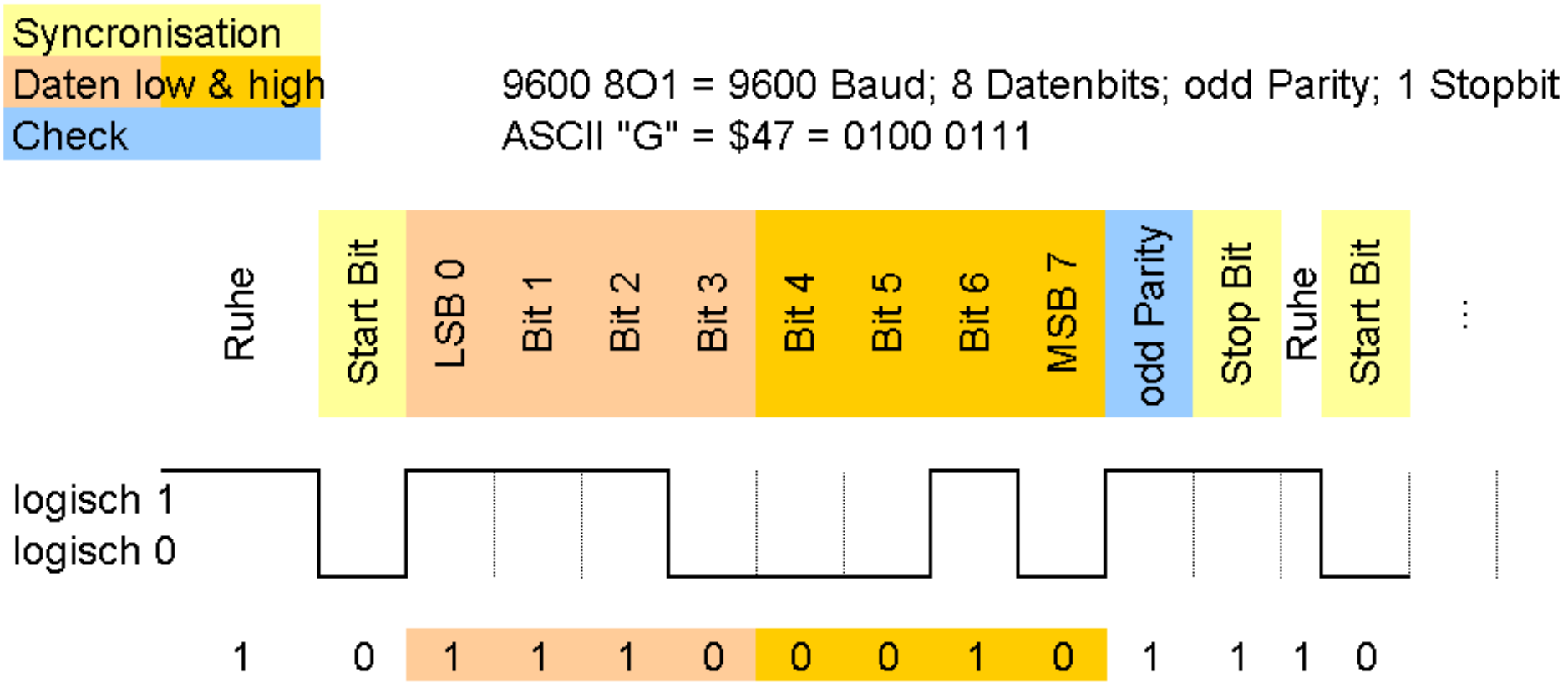
`http://nas.gus.tl/fpga/nexys4_micro_audioout_minimal.zip`



Datenblatt:

`http://www.ftdichip.com/Support/Documents/DataSheets/ICs/DS_FT2232H.pdf`

`https://de.wikipedia.org/wiki/Universal_Asynchronous_Receiver_Transmitter`



PC Software:

Realterm `http://realterm.sourceforge.net`

CuteCom `http://cutecom.sourceforge.net`

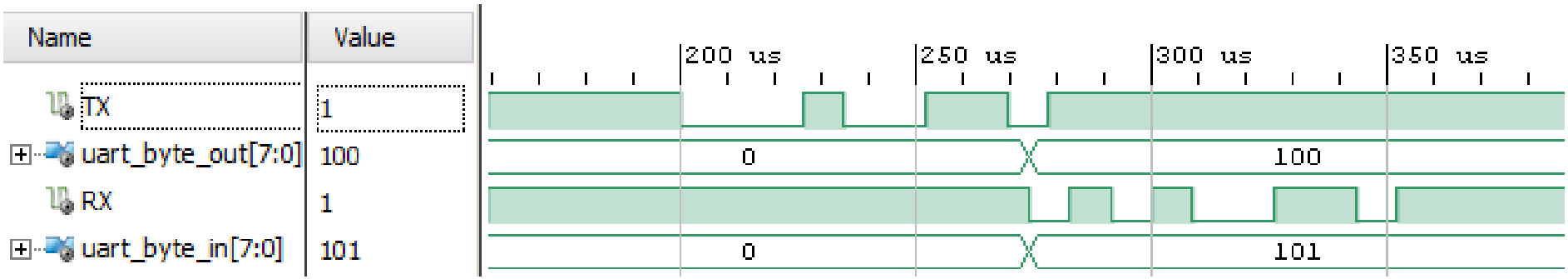
Pyserial `https://github.com/pyserial/pyserial`

Minimalbeispiel:

- Bidirektional, 115200 Baud 8N1
- sendet das inkrementierte empfangene Byte

Code:

`http://nas.gus.tl/fpga/nexys4_uart_minimal.zip`



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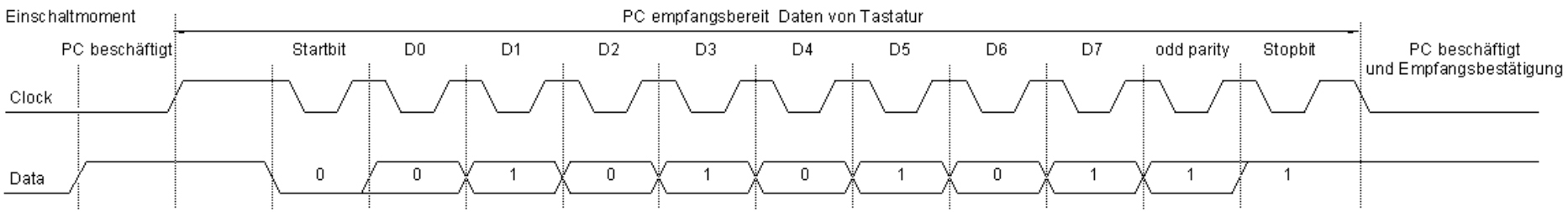
Keyboard Scan Codes:

Set 2 (Make und Break)

`http://computer-engineering.org/ps2keyboard/scancodes2.html`

Timing:



```
process begin
    wait until rising_edge(clk);
    sr <= sr(1 downto 0) & PS2_CLK;
    start <= '0';

    if sr(1) = '0' and sr(2) = '1' then -- falling_edge
        edgecounter <= edgecounter +1;
        bits(edgecounter) <= PS2_DATA;
        if edgecounter = 10 then
            edgecounter <= 0;
            start <= '1';
            byte <= bits(8 downto 1);
        end if;
    end if;
end process;
```

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Datenblatt:
`http://www.analog.com/media/en/technical-documentation/data-sheets/ADT7420.pdf`
(besonders die Seiten 12 und 19)

Erklärung zu I2C:
`http://www.ralph.timmermann.org/elektronik/i2c.htm`

Zweierkomplement:
`https://de.wikipedia.org/wiki/Zweierkomplement`
Rechner:
`http://manderc.com/concepts/umrechner`

Ablauf:

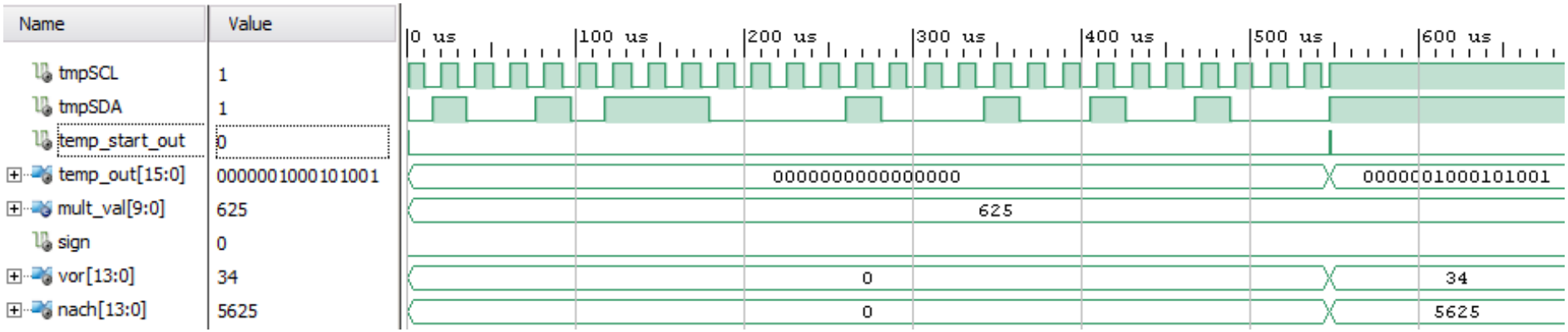
- Adresse "01001011" senden, R/W Bit setzen, ACK beachten.
- Zwei Bytes lesen, jeweils ACK/NACK setzen.
- 16-Bit Wert (Vorzeichen und 12 Bit Temperatur) umwandeln.

Minimalbeispiel:

- liest Temperatur und gibt sie als normale Dualzahl auf LEDs aus.
- `LED(15)` ist Vorzeichen
- `LED(11 downto 4)` ist Vorkomma
- `LED(3 down to 0)` ist Nachkomma, $\times 0{,}0625$ ergibt Dezimalzahl

Code:

`http://nas.gus.tl/fpga/nexys4_temp_minimal.zip`



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Datenblatt:
`http://www.analog.com/media/en/technical-documentation/data-sheets/ADXL362.pdf`
(besonders die Seiten 19, 20, 23 und 26)

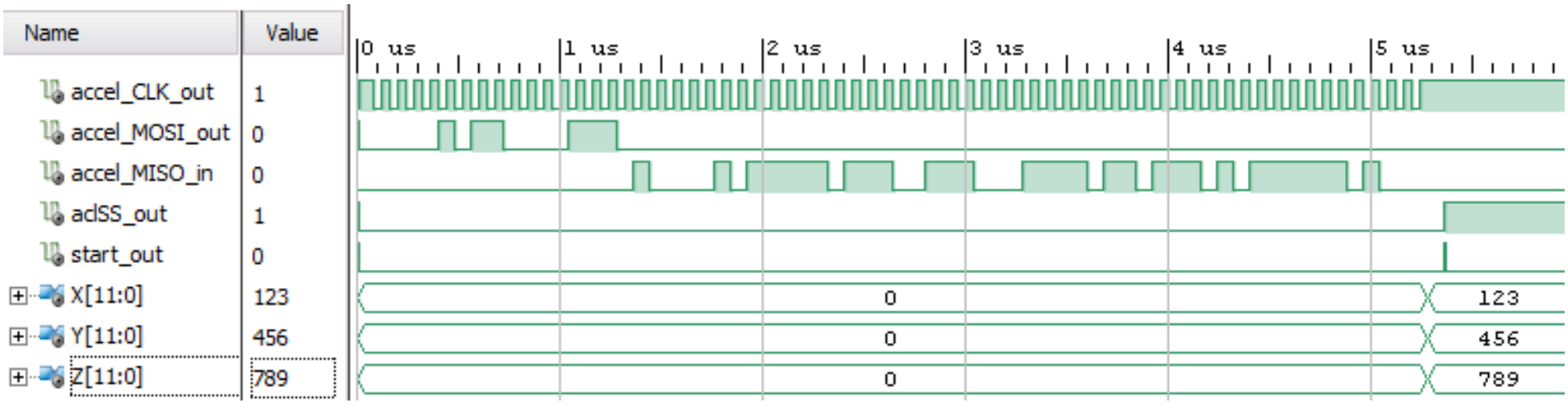
Ablauf:
- SPI Command `x0B` (read) senden, Startadresse `x0E` (`XDATA_L`) senden.
- Adresse wird automatisch erhöht
- 48 Bits lesen, zerlegen in X, Y, und Z
- Werte umwandeln/verarbeiten

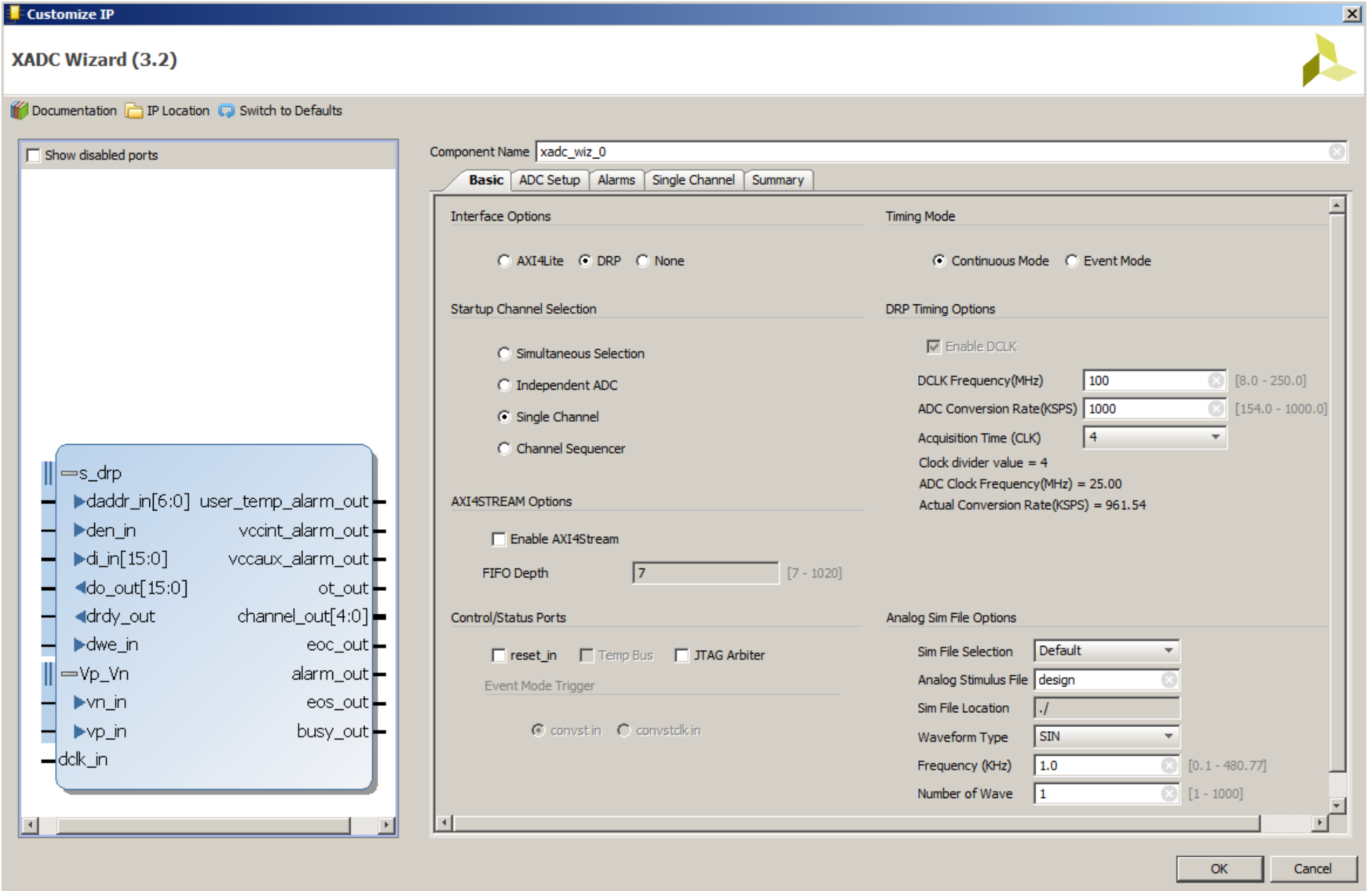
Komponente:

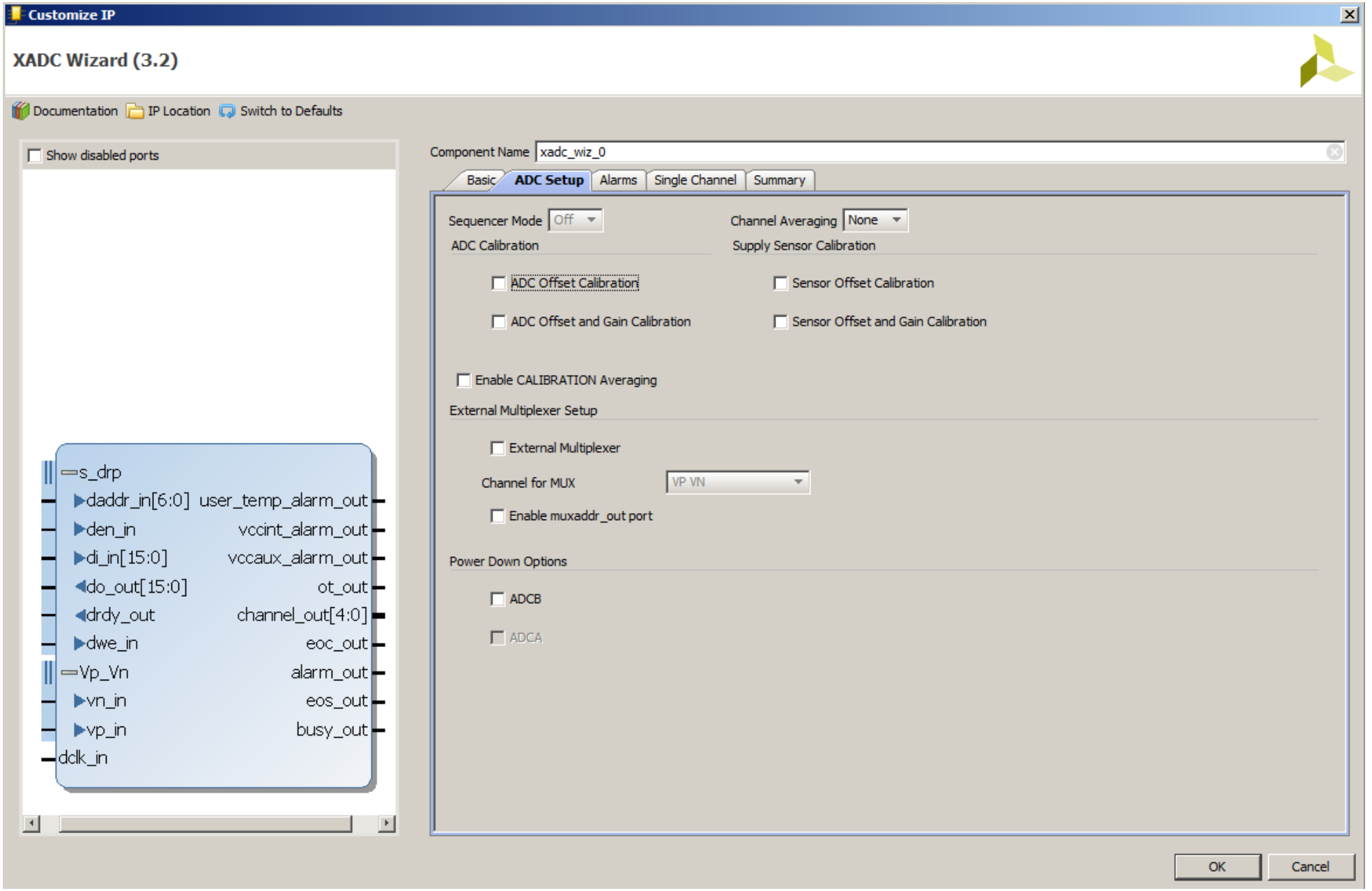
- liest X, Y und Z Wert mit ca. 95 Hz Updaterate
- Ausgabe als 12 Bit Dualzahl

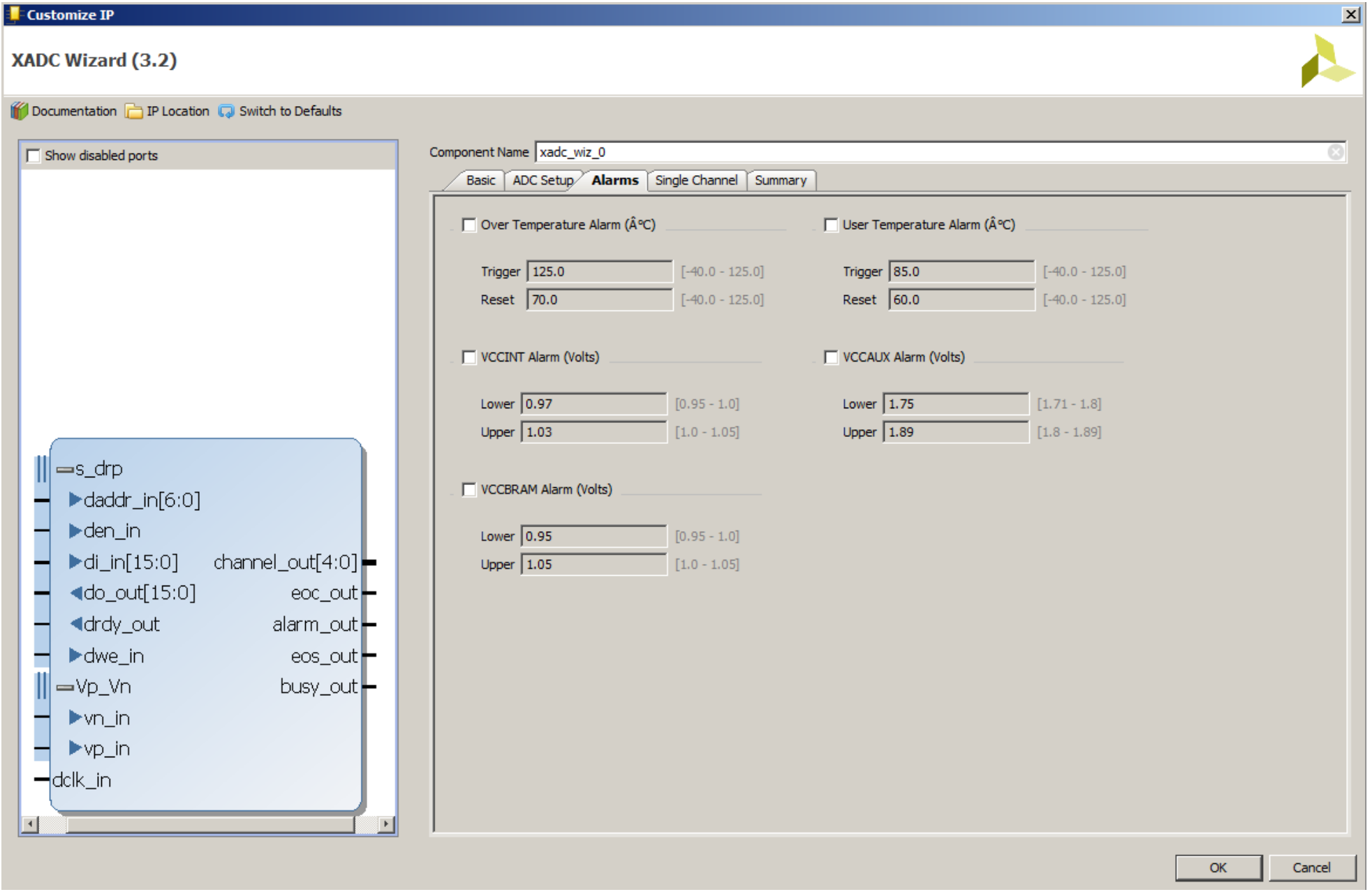
Code:

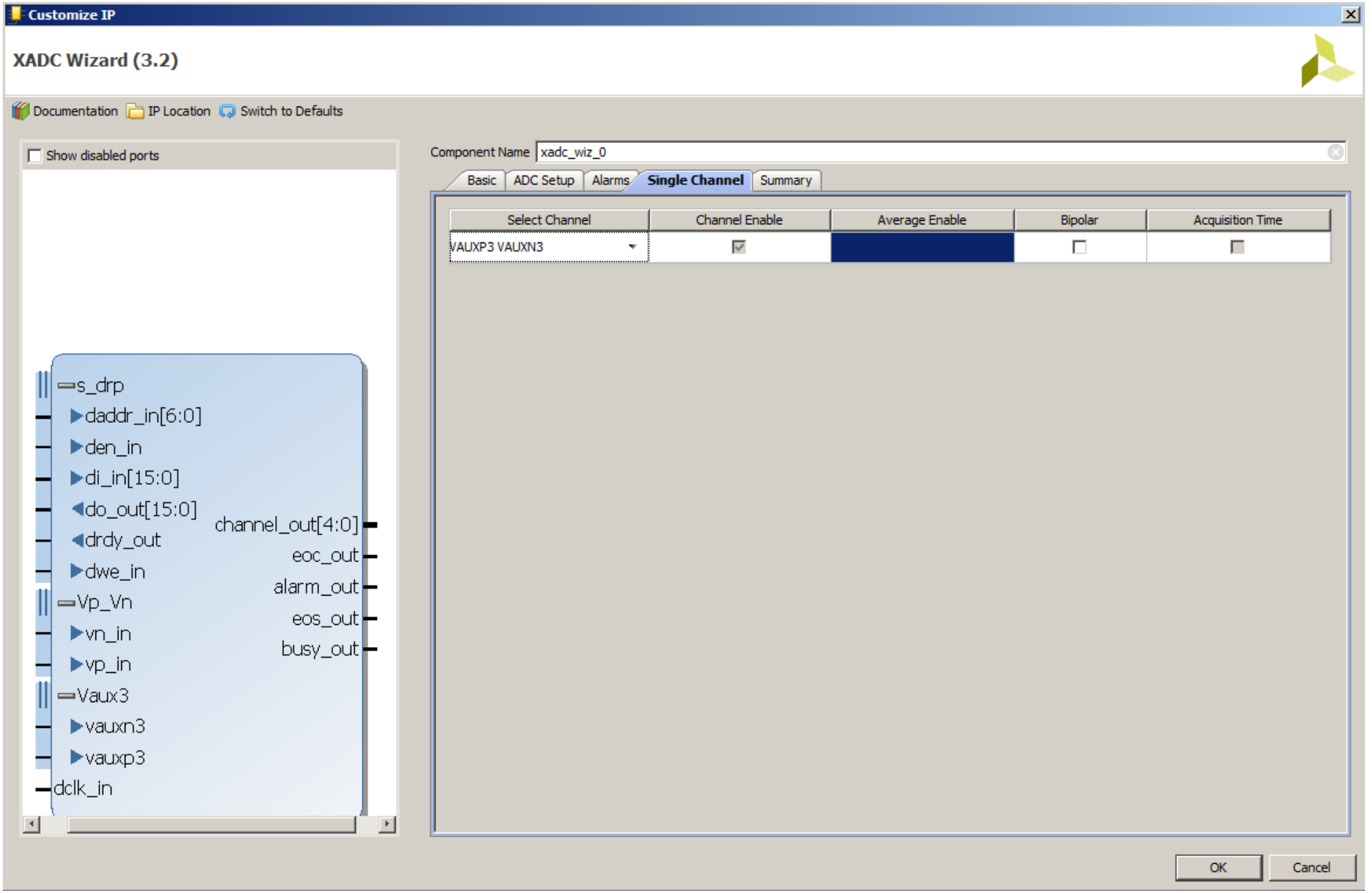
`http://nas.gus.tl/fpga/nexys4_accel_sim.zip`




Customize IP
XADC Wizard (3.2)
Documentation
IP Location
Switch to Defaults
Show disabled ports
s_drp
daddr_in[6:0]
den_in
di_in[15:0]
do_out[15:0]
drdy_out
dwe_in
Vp_Vn
vn_in
vp_in
dclk_in
user_temp_alarm_out
vccint_alarm_out
vccaux_alarm_out
ot_out
channel_out[4:0]
eoc_out
alarm_out
eos_out
busy_out
Component Name
xadc_wiz_0
Basic
ADC Setup
Alarms
Single Channel
Summary
Interface Options
AXI4Lite
DRP
None
Timing Mode
Continuous Mode
Event Mode
Startup Channel Selection
Simultaneous Selection
Independent ADC
Single Channel
Channel Sequencer
DRP Timing Options
Enable DCLK
DCLK Frequency(MHz)
100
[8.0 - 250.0]
ADC Conversion Rate(KSPS)
1000
[154.0 - 1000.0]
Acquisition Time (CLK)
4
Clock divider value = 4
ADC Clock Frequency(MHz) = 25.00
Actual Conversion Rate(KSPS) = 961.54
AXI4STREAM Options
Enable AXI4Stream
FIFO Depth
7
[7 - 1020]
Control/Status Ports
reset_in
Temp Bus
JTAG Arbiter
Event Mode Trigger
convst in
convstclk in
Analog Sim File Options
Sim File Selection
Default
Analog Stimulus File
design
Sim File Location
./
Waveform Type
SIN
Frequency (KHz)
1.0
[0.1 - 480.77]
Number of Wave
1
[1 - 1000]
OK
Cancel


Customize IP
XADC Wizard (3.2)
Documentation
IP Location
Switch to Defaults
Show disabled ports
s_drp
daddr_in[6:0]
den_in
di_in[15:0]
do_out[15:0]
drdy_out
dwe_in
Vp_Vn
vn_in
vp_in
dclk_in
user_temp_alarm_out
vccint_alarm_out
vccaux_alarm_out
ot_out
channel_out[4:0]
eoc_out
alarm_out
eos_out
busy_out
Component Name
xadc_wiz_0
Basic
ADC Setup
Alarms
Single Channel
Summary
Sequencer Mode
Off
Channel Averaging
None
ADC Calibration
Supply Sensor Calibration
ADC Offset Calibration
Sensor Offset Calibration
ADC Offset and Gain Calibration
Sensor Offset and Gain Calibration
Enable CALIBRATION Averaging
External Multiplexer Setup
External Multiplexer
Channel for MUX
VP VN
Enable muxaddr_out port
Power Down Options
ADCB
ADCA
OK
Cancel


Customize IP
XADC Wizard (3.2)
Documentation
IP Location
Switch to Defaults
Show disabled ports
s_drp
daddr_in[6:0]
den_in
di_in[15:0]
do_out[15:0]
drdy_out
dwe_in
Vp_Vn
vn_in
vp_in
dclk_in
channel_out[4:0]
eoc_out
alarm_out
eos_out
busy_out
Component Name
xadc_wiz_0
Basic
ADC Setup
Alarms
Single Channel
Summary
Over Temperature Alarm (Â°C)
Trigger 125.0 [-40.0 - 125.0]
Reset 70.0 [-40.0 - 125.0]
User Temperature Alarm (Â°C)
Trigger 85.0 [-40.0 - 125.0]
Reset 60.0 [-40.0 - 125.0]
VCCINT Alarm (Volts)
Lower 0.97 [0.95 - 1.0]
Upper 1.03 [1.0 - 1.05]
VCCAUX Alarm (Volts)
Lower 1.75 [1.71 - 1.8]
Upper 1.89 [1.8 - 1.89]
VCCBRAM Alarm (Volts)
Lower 0.95 [0.95 - 1.0]
Upper 1.05 [1.0 - 1.05]
OK
Cancel


Customize IP
XADC Wizard (3.2)
Documentation
IP Location
Switch to Defaults
Show disabled ports
s_drp
daddr_in[6:0]
den_in
di_in[15:0]
do_out[15:0]
drdy_out
dwe_in
Vp_Vn
vn_in
vp_in
Vaux3
vauxn3
vauxp3
dclk_in
channel_out[4:0]
eoc_out
alarm_out
eos_out
busy_out
Component Name
xadc_wiz_0
Basic
ADC Setup
Alarms
Single Channel
Summary
Select Channel
Channel Enable
Average Enable
Bipolar
Acquisition Time
VAUXP3 VAUXN3
OK
Cancel

Datenblatt:

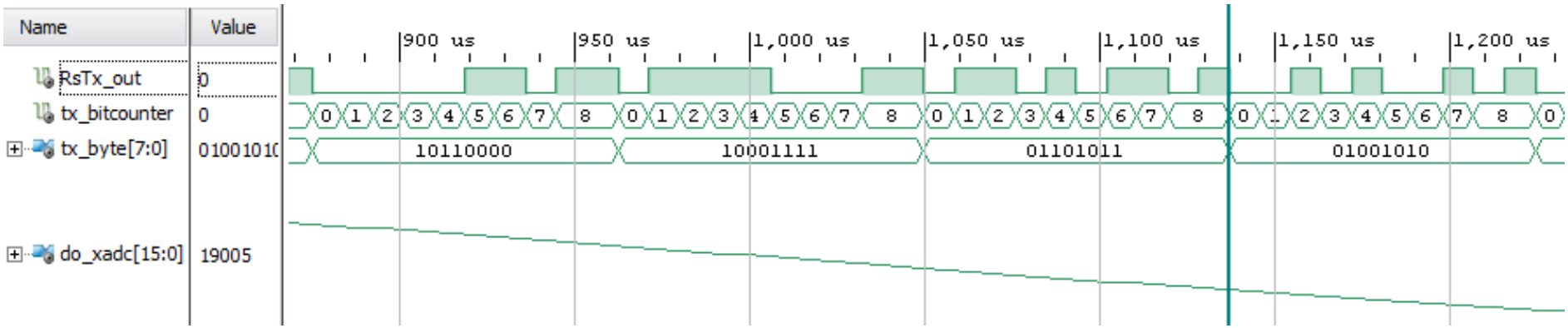
`http://www.xilinx.com/support/documentation/user_guides/ug480_7Series_XADC.pdf`
(besonders die Seiten 18, 19, 20, 38 und 75)

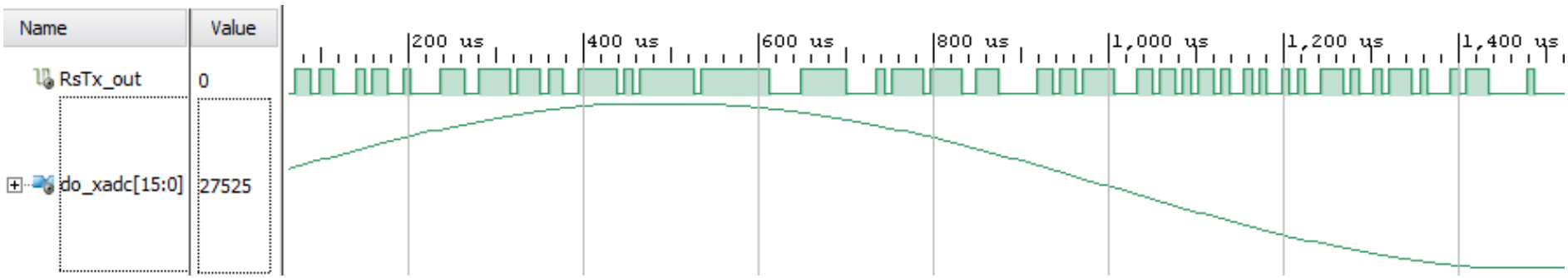
Minimalbeispiel:

- Analoge Anschlüsse dürfen nicht in der .ucf/.xdc beschrieben werden.
- In der Testbench analoge Anschlüsse auf 'Z' legen.
- Für die Simulation das erzeugte `design.txt` samt Pfad in die generierte `xadc_wiz_0.vhd` bei `SIM_MONITOR_FILE` eintragen.
- `VAUXP3` $\Longrightarrow$ `JXADC(0)`, Pin 1 auf dem Board: `AD3P`
- `VAUXN3` $\Longrightarrow$ `JXADC(4)`, Pin 7 auf dem Board: `AD3N`
- Ein- und Ausgänge (derselben Bank) auf `IOSTANDARD LVCMOS18` setzen.
- liest Daten aus Register 19 (`VAUXP3` und `VAUXN3`)
- sendet Daten über UART 115200 Baud 8N1

Code:

`http://nas.gus.tl/fpga/nexys4_xadc_minimal.zip`





Fragen?

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